Abstract

A method is used to make a bit selectable device having nanotube memory elements. A structure having at least two transistors is provided, each with a drain and a source with a defined channel region therebetween, each transistor further including a gate over said channel. A trench is formed between one of the source and drain of a first transistor and one of the source and drain of a second transistor. An electrical communication path is formed in the trench between one of the source and drain of a first transistor and one of the source and drain of a second transistor. A defined pattern of nanotube fabric is provided over at least a horizontal portion of the structure and extending into the trench. An electrode is provided in the trench. A pattern of nanotube fabric is suspended so that at least a portion is vertically suspended in spaced relation to the vertical walls of the trench and positioned so that the vertically suspended defined pattern of nanotube fabric is electromechanically deflectable into electrical communication with one of the drain and source of a first transistor and one of the source and drain of a second transistor.